Implementation of FPGA based 3-Phase Inverter FED BLDC Motor

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Abstract: Advance in Power Electronics has led to an increased interest in three-phase inverters with PWM control of ac drives. Most of the AC drives and Universal PWM inverters in use today are adapting microprocessor based digital control strategy. Field Programmable Gate Arrays (FPGA) is increasingly being used in motor control applications due to their robustness and customizability. FPGA implementation has the capability of executing several processes in parallel. Hence, the total control of the inverter together with the motor can be implemented in a single FPGA chip [1]. The use of Pulse Width Modulation (PWM) in power electronics to control high energy with maximum efficiency & power saving is not new but, interesting is to generate PWM signals using Hardware Descriptive Language (HDL) and implementing it in FPGA [3],[7]. FPGA implementation of PWM is selected because it has provided an economic solution & fast circuit response due to its simultaneous instead of sequential execution. In this paper the FPGA based controller for BLDC motor is an experimental model implementation of Sinusoidal PWM strategy (SPWM) control scheme. The proposed control scheme can be realized and the Simulation results are verified using FPGA SPARTAN-3A DSP Trainer kit from Xilinx with the help of VHDL programming algorithm of digital PWM Generator topology.

Keywords: BLDC Motor, Field Programming Gate Array (FPGA), Sinusoidal PWM (SPWM), VHDL, Voltage Source Inverter (VSI).

Introduction:
Now-a-Days, Brushless DC (BLDC) motors are one of the electrical drives that are rapidly gaining popularity, due to their high efficiency, good dynamic response and low maintenance and are widely used in many motor applications developing high torque with good speed response.

The speed of the motor is directly proportional to the applied voltage. By varying the average voltage across the windings, the speed can be altered. This is achieved by altering the duty cycle of the base PWM signal. PWM Inverters are mostly used for industrial applications because of their superior performance.

The use of PWM in power electronics to control high energy with maximum efficiency & power saving is not new but, interesting is to generate PWM signals using HDL and implementing it in FPGA [1], [5].

The paper presents the simulation of the speed control of BLDC motor, which can be done using the software XILINX with the help of VHDL programming. An FPGA based speed controller is designed for closed loop operation of the BLDC motor so that the motor runs much close to the reference speed.

Methodology:
A. Principle of Operation
Brushless DC Motors are a type of Synchronous motor. This means that the magnetic field generated by the stator & the rotor rotate at the same frequency. These motors do not experience the “Slip” that is normally seen in Induction Motors. The construction of modern Brushless motors is very similar to the AC Motor, known as the Permanent Magnet Synchronous Motor (PMSM). Brushless DC motors usually consist of three main parts: Stator, Rotor and Hall Sensor.

- Stator which consists of three coils each including three elements in series, an inductance, a resistance and one back electromotive force. In many motors the number of coils is replicated to have a smaller torque ripple.
- A Rotor which consists of an even number of permanent magnets. The number of magnetic poles in the rotor also affects the step size and torque ripple of the motor. More poles give smaller steps and less torque ripple.
- Hall Sensors are placed every 120° for the estimation of the rotor position in the motor

Brushless DC motors are used in a growing number of motor applications as they have many advantages:
1. They have no brushes so they require little or no maintenance.
2. They generate less acoustic and electrical noise than universal brushed DC motors.
3. They can be used in hazardous operation environments (with flammable products).

B. Proposed Topology of BLDC Motor

The block diagram of the proposed system is shown in Fig.1. The drive system consists of a 3 phase AC supply, 3 phase Diode bridge Rectifier, 3 phase six switch Inverter, Brushless DC Motor and controlled circuits (Xilinx processor and Driver circuit).
The standard AC power supply is converted to a DC by using a 3-phase diode bridge rectifier. A voltage source Inverter is used to convert the DC voltage to the controlled AC voltage. The output of Inverter is fed to Brushless DC motor [4]. VHDL program is used in Xilinx software to generate the controlled PWM pulses at different duty ratio for Inverter to drive the Brushless DC Motor at different speeds [6].

Hardware Implementation Using FPGA:

A. Experimental Set-Up

The power circuit of the Voltage Source Inverter fed BLDC Motor drive is shown in Fig. 2. The inverter has six switches, S1, S2, S3, S4, S5 and S6 and a DC Link connected to a Diode Bridge Rectifier [2].

B. System Description

A complete overview of the system can be seen on Fig. 2, which includes the FPGA, a three phase inverter, a Brushless DC motor, and a linear encoder attached to the motor [2]. The entire System is interfaced through a PC. PC acts a Man-Machine Interface in which the user can set the reference speed of the motor, and read the actual speed.

Functions of FPGA:

FPGAs are increasingly being used in motor control applications due to their robustness and customizability. Microcontrollers have typically been used to implement motor controls, with computation algorithms executed by software. Some of the challenges in this implementation are response time, a fixed number of PWM channels, limited communication interfaces and pre-determined analog triggering. The solution is to use an FPGA. Since, the performance of the FPGA has not been fully utilized, the combination of FPGA & DSP is the conventional control scheme used for the motor control. The FPGA acts as a buffer for PWM generation unit of the DSP. The tasks taken by FPGA & DSP were divided according to the functions needed in motor control [1], [7]. The functions taken by FPGA include- generating the PWM signals, calculating of motor rotational speed, generating the phase conversion control signals, data exchanging between FPGA & DSP and calculation of current loop where as the function taken by DSP include calculation of rotational speed loop and receiving speed instruction [3], [7].

PWM generation using FPGA

PWM signals are generated from the Spartan-3A processor by writing VHDL program to control the inverter switches [3], [4]. The switching signal parameters namely switching frequency, the duty ratio and the number of pulses are easily controlled via VHDL programming language.

A. Principle of generating PWM

The principle of generating PWM waveform is shown in Fig.3.Bidirectional counter is used to generate triangular wave. The value of compare register is compared with triangular wave. If the value of compare register is less than the value of triangular wave, then PWM is ‘1’, else PWM is ‘0’[1],[4].

FPGA implementation of PWM is selected because FPGA has provided an economic solution & fast circuit response due to its simultaneous instead of sequential execution [3].

B. Proposed Technique

Sinusoidal PWM (SPWM) technique is the proposed technique used to generate the PWM signals to the VSI in this paper. SPWM is based on the comparison of a sinusoidal control signal with a triangular carrier. The switches on a single branch are turned on or off depending on whether the control signal is greater or smaller than the carrier. Working with three phase loads, the control signals must be standard three phase sine waves.

The signals, $P_R$, $P_Y$, $P_B$, (Fig.4b) generated by comparison of one triangular with three sine waves (Fig. 4a), are directly used to drive the switches of each leg of the VSI are shown in figure 4.
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HDL Code Generation:
Writing VHDL is tedious and the hand written code still needs to be verified with Simulink and Simulink HDL coder, once we have simulated the model we can generate VHDL directly and prototype an FPGA. It also saves a lot of time and the generated code contains optimizations we hadn’t thought of.

A. Xilinx ISE Software Overview
The ISE Design Suite is the Xilinx design environment which allows us to take the design from design entry to Xilinx device programming [6]. The figure 5 shows the flow chart of FPGA design and embedded in a single chip for generating gate signals to drive the three phase inverter.

The corresponding VHDL program code is generated from the Simulink HDL Coder after verification and simulation of the design. The VHDL program is verified and simulated using Xilin-ISE 12.1 software.

The FPGA design flow comprises the following steps:
1. Design entry – it should assign constraints such as timing, pin location, and area constraints, including user constraints (UCF) file.
2. Design synthesis- Synthesize the project design.
3. Design implementation- Implement the design which includes the Translate, Map, Place and Route.
4. Design verification- includes both functional verification (also known as RTL simulation) and timing verification.
5. Xilinx® device programming- Create a programming BIT file program debugging or to download to target device of XILINX/SPARTAN-3A processor kit.

Once the program is dump to FPGA kit, it acts as a controller and generates gate signal

B. Algorithm for Generating PWM Pulses
The algorithm for generating PWM pulses by using SPWM technique is given in following steps:
1. Initializing the inputs and the outputs.
   i. Inputs- Clock, Frequency and Amplitude
   ii. Output-Pulses
2. Declaring Capturing Signals a, b, c.
3. Interrupt is given based on Capture Values.
4. Declaring the array of 256 Sine values.
5. Let xx=Carrier Signal yy=Comparing Value
6. From the Ramp signal, C, triangular wave is generated.
7. Compare Sine values with the Triangular wave
8. Pulses are generated.
9. Now set the Frequency and Amplitude of Carrier and Sine.

Simulation and Experimental Results:
Digital computer simulation model of 3-Phase Voltage Source Inverter fed BLDC motor drive has been developed by using XILINX 12.1.[1],[5],[6].The Simulation work has been performed for this drive system and the HDL code is written for generating PWM pulses using SPWM technique. The generated code is simulated and the verified generated HDL code is observed with the Mentor Graphics Model-Sim Simulator. The Simulation results observed in Model-Sim Simulator are as shown in figure 6(a), 6(b)

Fig 6(a), (b): Simulation results of SPWM
In the Experimental work the components used are an FPGA board, Personal Computer, Inverter module, and BLDC motor, as shown in Fig.1. The IGBT Inverter module consists of Converter, Driver circuit, Split capacitor and Driver circuit as shown in Fig.2. The generated PWM pulses observed in the digital CRO are as shown in figure 7(a), 7(b).

Figure 9 shows the Fluke Meter readings of voltage and current of the Inverter Module.

The Inverter module outputs are measured by using a Fluke Meter while performing the experiment on the set-up. Figure 8 shows the waveform of output voltages of the inverter module observed in the Fluke Meter.

The graphs between the Set Speed and the Actual speed for the forward and reverse direction are observed in the PC for the closed loop operation of the BLDC Motor at different loads.

The Speed response of a closed loop BLDC Motor in forward direction is shown in figure 10.

Figure 11 shows the Speed response of a Closed Loop BLDC Motor in Reverse Direction.

The Hardware details of the experimental set-up are tabulated in the Table-1.
Table 1: Hardware Details

<table>
<thead>
<tr>
<th>Components</th>
<th>Ratings</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Board</td>
<td>1.Xilinx XC3SD1800A-FG676-4 Spartan 3A DSP FPGA</td>
</tr>
<tr>
<td></td>
<td>2.16×2 LCD interface</td>
</tr>
<tr>
<td></td>
<td>3.ADC &amp; DAC interface</td>
</tr>
<tr>
<td></td>
<td>4.USB 2.0 Compliant interface (480 Mbits/sec)</td>
</tr>
<tr>
<td>Inverter Module</td>
<td>IGBT:25A,1200V,Driver Circuit, 3-Phase Diode Bridge Rectifier, Vin=400I=220mA</td>
</tr>
<tr>
<td>BLDC Motor</td>
<td>4600 rpm @ 310 Vdc</td>
</tr>
</tbody>
</table>

Conclusion:
This paper presents the design of FPGA Controller for BLDC motor drive. An FPGA based implementation of Voltage Source fed BLDC Motor drive using PWM control is successfully carried out in simulation and real-time experiment. XILINX 12.1 is used for simulation where the Simulation results observed in Model-Sim Simulator and the hardware implementation is carried out using SPARTAN-3A processor. VHDL (Very high speed description language) program is developed in XILINX to generate the controlled PWM pulses to drive the system [1], [5].

References: